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Hardware-in-the-loop Wide Area Monitoring Protection and Control Using Software based PMU's Model

*Md Hazzaz Mahmoud, Mohammad Reza Barzegaran**

Department of Electrical Engineering, Lamar University, Texas, USA

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Phasor measurement units (PMUs),
Smart grid,
Wide area measurement system (WAMS).

Abstract

With the growth of power system both in terms of geographical as well as technological advancement, it requires tools for dealing with system-wide disturbances that often cause widespread blackouts in power system networks. When any kind of fault or major disturbance occurs, protection and control measures play the vital role to prevent further degradation of the system, restore the system back to a normal state. Continuous technological innovation in information and communication technology, various kind of sensors and measurement instrument principle in general have promoted the advent of phasor measurement units (PMU). This paper describes the modeling and testing of phasor measurement units through Hardware in the loop implmementation with Simulink and the combination of two powerful microcontroller. Since PMU are costly device so module based analysis is not desired. That's why software based analysis are appreciable. These has been done through MATLAB and results are analyzed.

1. Introduction

The incidents of major blackouts in many power system around the world have given a new impetus for large scale implementation of wide area measurement system (WAMS) [1]. In smart grid, communication based controlling and monitoring architecture is used to save power and increase stability and reliability. The WAMS has been used in measuring devices, which have their own clocks synchronized with the common time reference using synchronizing devices. This concept is not new and for many years radio signals sent from ground stations have been used. In preceding systems, many supervisory control and data acquisition (SCADA) systems, which are used for monitoring and control of power system operation, utilize the DCF77 signals for synchronization. The time delay of conventional synchrophasors which use DCF77 [2] are 1-10ms which is half of a 50Hz cycle. Since the main duty of the system is real-time monitoring for control

* Corresponding Author:
E-mail, *barzegaran@lamar.edu* – Tel, (+1) 4098807593 – Fax, (+1) 4098808121

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and protection as well as self-healing purposes, the delay is very crucial. Presently much better precision, at least 1 μs, is obtained using satellite GPS (Global Positioning System).

The accuracy of the GPS reference time of about 1 μs is good enough to measure AC phasors with a frequency of 60 Hz which is small enough with high accuracy from the point of view of phasor measurement. This accuracy brought up the opportunity to integrate the WAMS with WAM, WAP and WAC which is referred to as wide area measurement, protection and control (WAMPAC). Recent years have seen a dynamic expansion of WAMPAC systems.

The technology component and platform (phasor measurement units, Data Concentrators, Data Acquisition systems, Communication Systems, EMS/SCADA, Market Operations Systems, etc.) required to implement a WAMPAC are already available. Measurement techniques and telecommunication techniques have made rapid progress, but the main barrier for the expansion of WAMPAC systems is a lack of WAP and WAC control algorithms based on the use of phasors. There has been a lot of research devoted to that problem but the state of knowledge cannot be regarded as satisfactory [3, 4].

PMUs as the core of WAMS measures the parameters from buses and components but the existing commercial PMUs are sophisticated and expensive. It is also very difficult to modify the program of them and their PDC. In addition, coordinating and matching them is difficult because they are not open source. These difficulties and the cost of the component as well as training discourages the industry to facilitate their system with these PMUs.

In the detail and technical point of view, the part in PMUs that needs improvement is in developing applications, specifically the software that operates on the data provided by the PMUs. Although academia, vendors, utilities, and consultants have developed a large number of methods and algorithms and performed system analysis and studies to apply the technology, similar to any other advanced tool, PMUs are good only in the hands of trained users. In addition to the above problems, the cost of the present commercial PMUs are the main issue. The reason for high cost is GPS requirement, and communication infrastructure requirement.

This research paper represents modular analysis of PMUs. This is essential to determine the functioning of individual modules within a PMU. MATLAB Simulink model is extensively used to implement the idea.The paper is divided into following major sections: Section II brief overview of PMU technology. Section III flow diagram of simulation model of PMU. Section IV perform case study and results. Section V conclusion and further work to do.

2. Brief Overview of PMU Technology

PMUs have been instrumental for interlinking of power system through wide area measurement system.

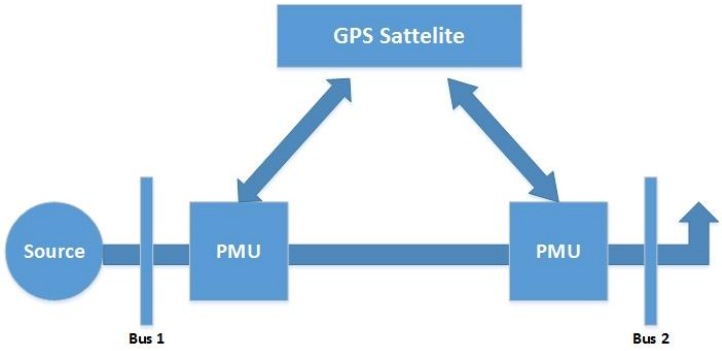

Figure 1. Phasor measurement at remote location

The PMUs in WAMS employ synchronous data collection hierarchy for real time monitoring of power system [5]. This is shown in Figure 1. The two PMUs at two buses provide time synchronized data. This helps for grading the currents and voltage signal using common reference signal obtained from GPS.

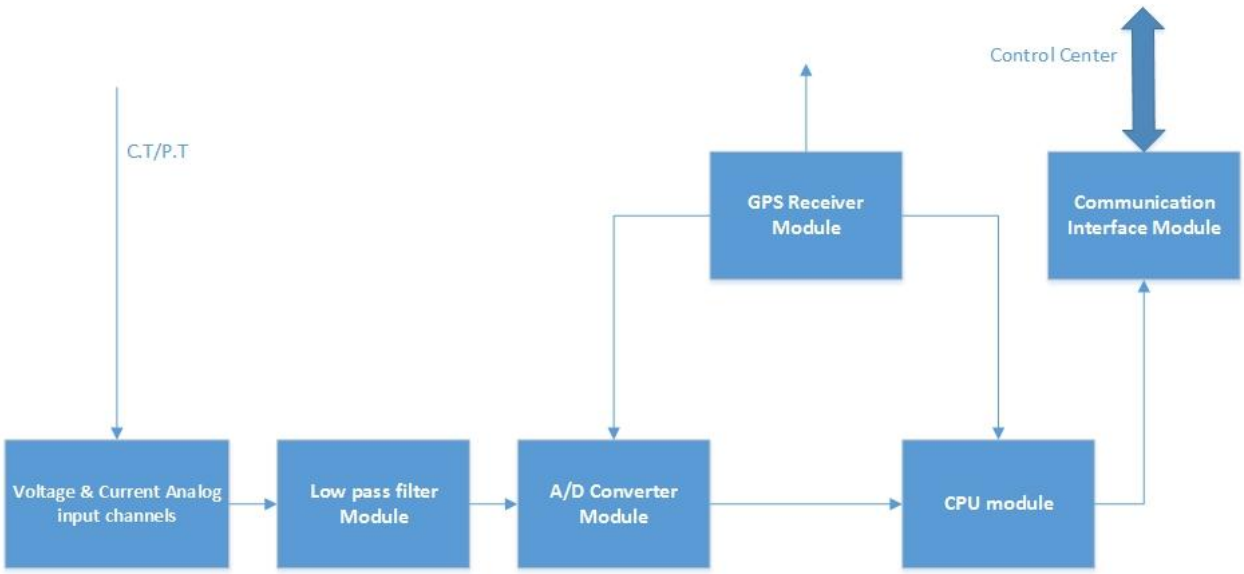

Figure 2. Fundamental representation of phasormeasurement unit

The figure shown in Figure 2 is the fundamental block representation of PMU. Here, Current and Voltages are coming from C.T and P.T. are going to the input channel block. The output of this block is going to low pass filter for removing higher order harmonics from the inputs. Then analog to digital converter block performs its operation. The measured voltages and currents and frequency are transmitted through GPS module and also could be saved in CPU.

3. Flow Chart for Simulation Model of PMU

In order to maintain accuracy in power system using PMU, an accurate model of PMU needs to be made. The flow chart for simulation of a PMU is given in Figure 3.

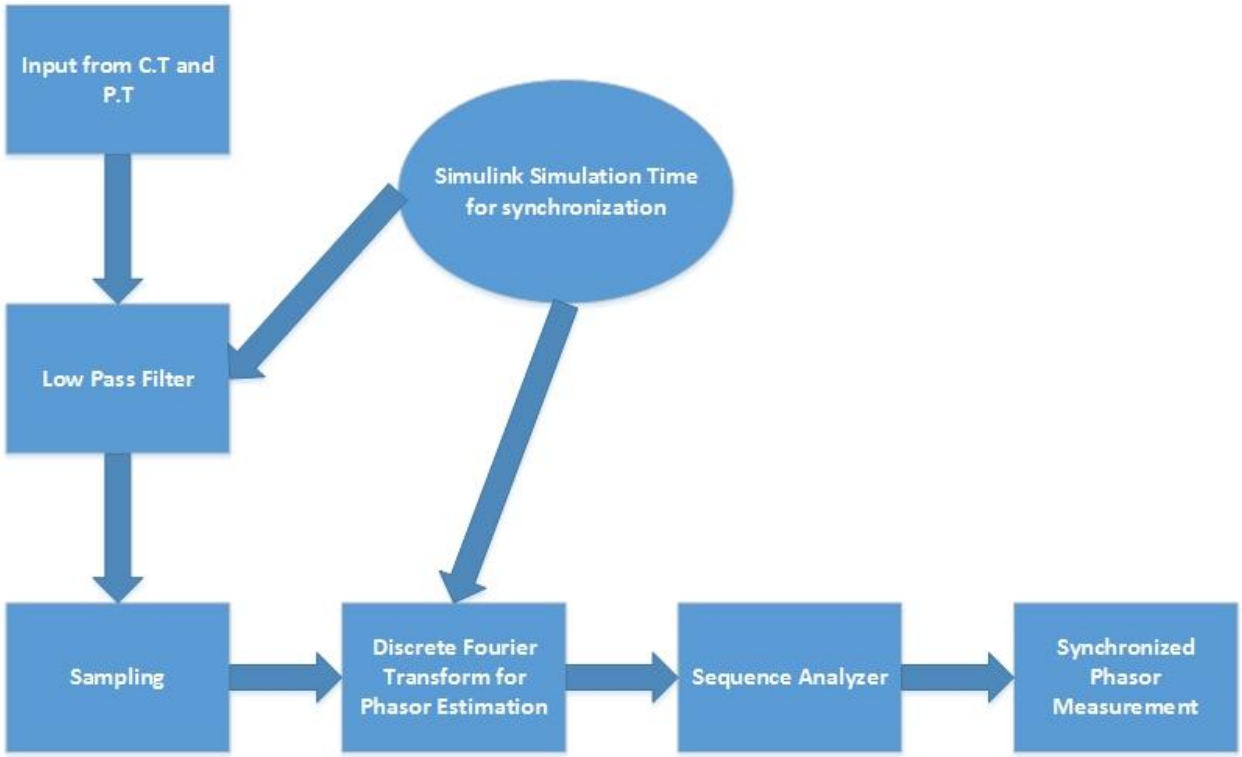

Figure 3. Simulation flow chart for PMU

The full cycle DFT is described as follows [6]

$$X = \frac{2}{N}\sum_{k=0}^{N-1} x_k e^{-j2\pi k/\mathrm{N}} \tag{1}$$

Prior to the discussion and results of PMU, for understanding properly lets go back to the conventional If asinusoidal signal of a known frequency *f* is fully described by its magnitude X_m and angular Φ with respect to an arbitrary time reference is applied as *X*, the phasor representation of the sinusoidal of above is given by $X = (X_m / \sqrt{2})\varepsilon^{j\phi}$. Accordingly, the measured positive sequence phasorwill be:

$$X'(k)_1 = PX(k)_1 \varepsilon^{jk(w-w_o)t} \tag{2}$$

where the coefficient *P* is given by

$$P = \left\{ \frac{\sin \frac{N(\omega - \omega_o)\Delta t}{2}}{N \sin \frac{(\omega - \omega_o)\Delta t}{2}} \right\} e^{j(N-1)\frac{(\omega-\omega o)\Delta t}{2}} \quad (3)$$

Here X is complex phasor, X_k is the sample discrete data of signal, and N is the number of samples per cycle.The positive, negative and zero sequence components of voltage or current are computed through sequence analyzer using the following equations [7].

4. Simulation Result and Discussion

A Simulink model of doubly fed two bus system is developed with PMUs as in Figure 4 with the following network parameters as given in Table 1.

Table 1. Network Parameters

Voltage Rating: 120k
System Frequency: 60Hz
Line Constant: Positive Sequence Resistance: 0.1153; Zero Sequence Resistance: 0.413; (ohm/km) Positive Sequence Inductance:1.05e-3; Zero Sequence Inductance: 3.32e-3; (H/km) Positive Sequence Capacitance: 11.33e-009; Zero Sequence Capacitance: 5.01e-009; (F/km)
Transmission Line length: 25km

Individual modules of PMUs are modeled to determine module wise output. The result of the output of both the PMUs are compared to analyze process. Simulink model includes various power system components which can be utilized for modeling of all kinds of power system network simulations.

The three phase input voltages are measured after each bus. These three phase voltage are given to the PMU and PMU gives us the positive, negative and zero sequence voltages and also the Angle. Figure 4 and 5 show the total Simulink model of WAMS.

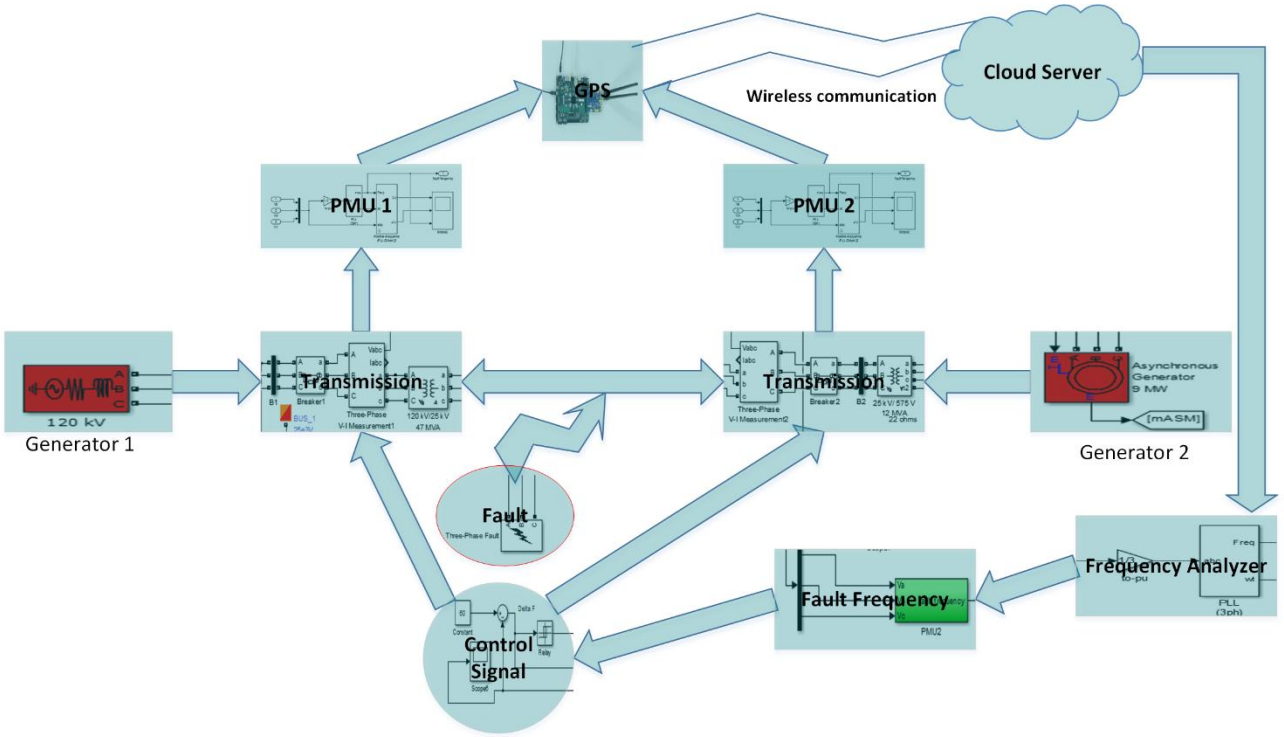

Figure 4. Schematic of the network with PMU during fault

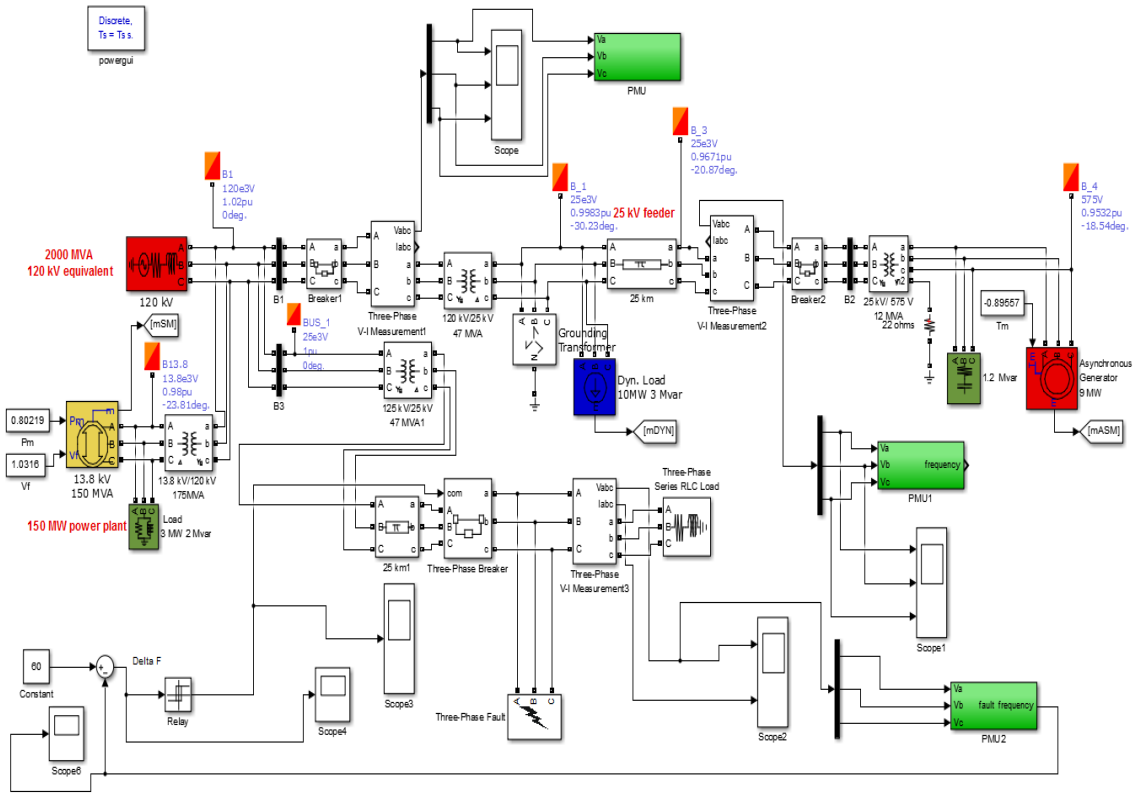

Figure 5. Simulation model for three bus system with PMU

Figure 6 illustrates clearing fault with feedback frequency from PMU that is compared with constant frequency 60 Hz and error signal is used to operate relay. The relay is used to switch on and off the three phase breaker. In designing the PMU, the dynamic of the system is considered, as

the transient after fault is visible in the figure. Moreover, the 3-phase voltage then measured by V-I measurement block and feed to the PMU block. PMU block is shown in Figure7, where the voltage feed into the Phase Locked Loop (PLL) and then sequence analyzer. That is how the three sequence voltage is built. Frequency can be measured through PLL. Figure 8 shows positive sequence voltage before, during and after fault. Figure 9 shows positive sequence angle at the same time frame and Figure 10 shows the frequency.

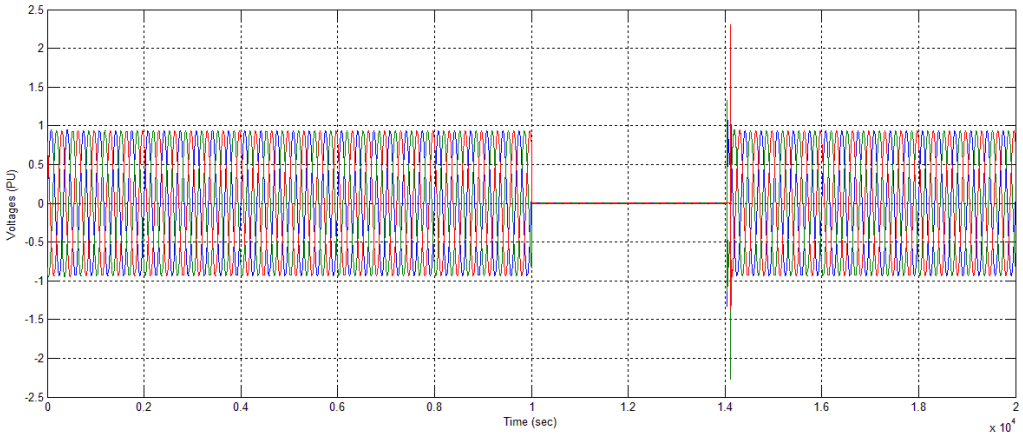

Figure 6. Voltage output after fault clearing using frequency feedback from PMU

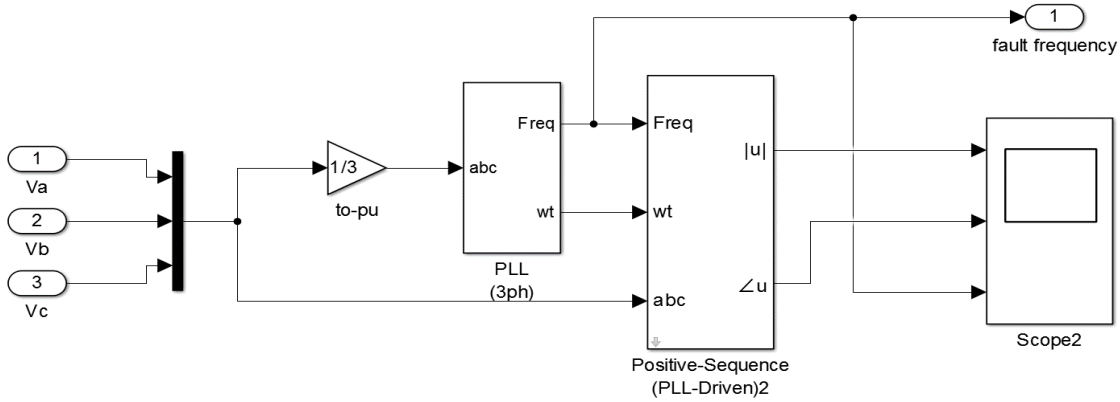

Figure 7. Phasor Measurement Unit

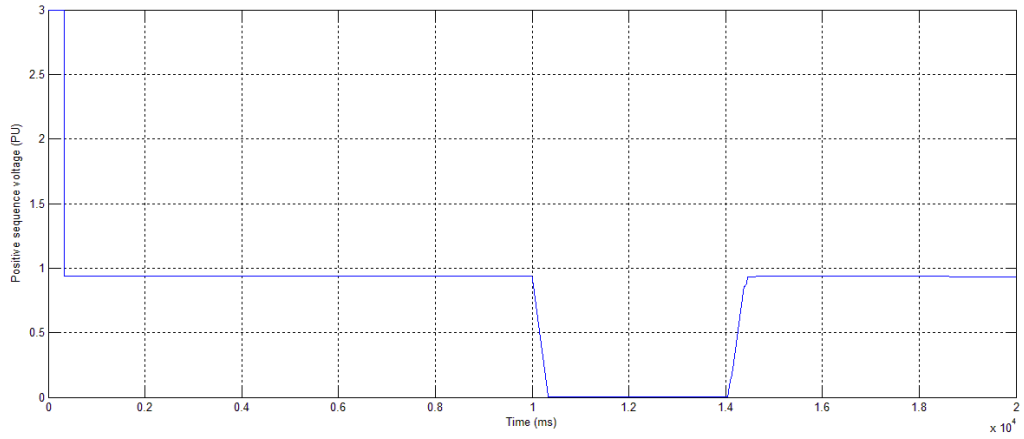

Figure 8. Positive sequence voltage

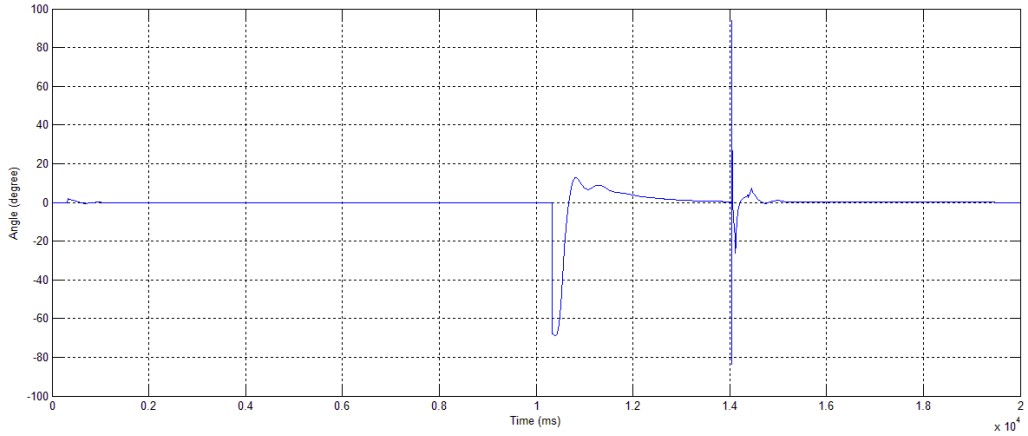

Figure 9. Positivesequence angle

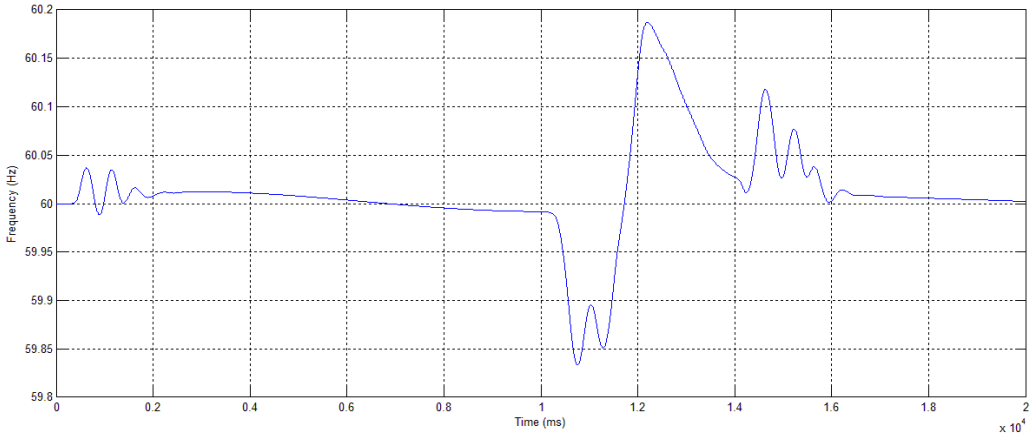

Figure 10. Frequency during before after and clearing fault

5. Hardware-in-the-loop Implementation (HIL)

The PMUs are the edifice for WAMS and their performance determines the performance of the WAMS for monitoring and control of modern power System. PMU is costly so hardware implementation needs precision in simulation. The hardware in the loop implementation of PMU can be implemented through specific microcontroller or FPGA within the simulation. In order to

select proper microprocessor, comparison between the best candidates, FPGA, STM32F4 Discovery Board and Texas Instrument Delfino F2833X Family are shown below.

Table 2. Comparison between FPGA, STM32F4 discovery board and texasinstrument delfino F2833X family

Distinctive	Field Oriented Programmable Gate Array (FPGA) Spartan-6	Texas Instrument Delfino F2833X Family	STM32F4 Discovery Board (ARM)
Overview	A FPGA board is made of thousands of configurable logic blocks (CBLs) as a matrix. These PBLs are entirely connected with each other and completely reprogrammable.	C2000 is a Real-time Control microcontrollers that brings leading floating-point performance and analog integration to real-time control applications.	STM32F4 is a microcontroller board by ST link.
Chip on board	Spartan 6 XC6SLX45	Dual-core C28x	ARM Cortex-M4F core
BIT	32-bit	32-bit	32-bit
I/O ports	Up to 576	Almost 176	75
Maximum Clock Speed	500MHz+ clock speeds*	200MHz for each core	32KHz
Flash memory	Up to 4.2MB	Up to 1MB	Up to 1MB
RAM	401 kB	Up to 204 kB	192 kB
Operating voltage	5V	%V	3.3V
Simulink Interface	Positive	Positive	Positive

*FPGA can be operated up to GHz range. Spartan-6 has up to six CMTs (Clock Management Tiles), each of them consisting of two DCMs (Digital Clock Managers) and one PLL (Phase Locked Loops). The most attractive side of Spartan 6 is that it has 16 global-clock lines which provide high fan out, short propagation delay and extremely low skew.

The FPGAs are programmed normally through direct HDL coding (Hardware Description Language) which is confusing, mainly if it is going to be programmed for large and complex applications such as smartgrid which needs active modification in programming for the purpose of protection and control. Moreover, programming ARM and interfacing with programming logic is another issue if arm is intended to be used. The other method which is appropriate for the application is adopting integrated hardware/ software workflow. The flowchart of this programming is shown in Figure 11.

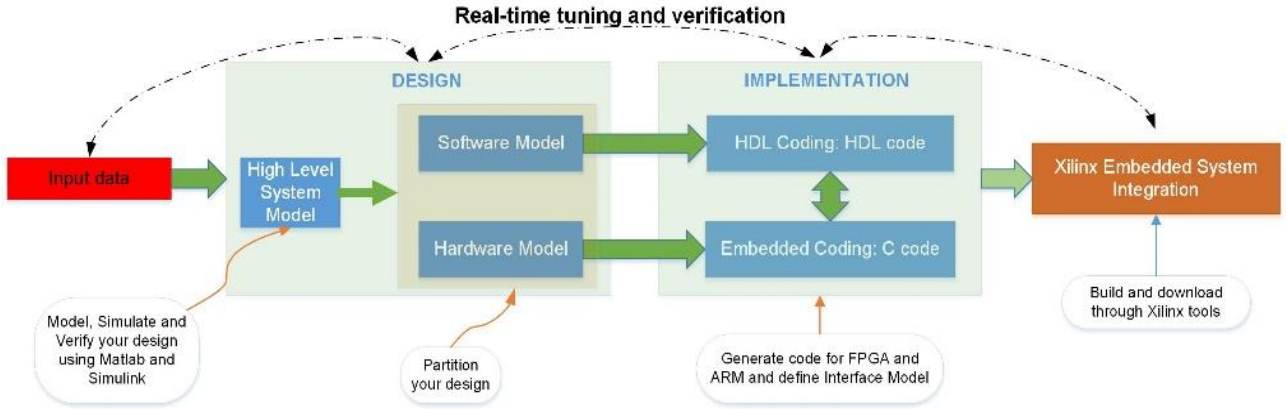

Figure 11. Integrated workflow of programming phasor measurement unit processor

This method is established on model based design approach. The input data with all requirements will be imported from data acquisition to the design block. The modeling, simulation and verification of the design are implemented using MATLAB and Simulink. Based on the complexity and the structure of design, some tasks will be implemented on processing system (ARM) and some will be implemented on programming logic (FPGA). The programming of processor and FPGA will be done automatically through embedded coder and HDL coder respectively, while the interface is established between them. Accordingly, the application will be built and run in the systrm including the ability to interact the board in real-time with the Simulink [8].

The proposed synchro-phasors is tested to determine its compliance with IEEE C37.118.1 standard as described in [9]-[10]. IEEE C37.118.1-2011 describes tests for compliance throughout steady state circumstances and, further to the 2005 version of the standard, also includes dynamic conditions and Total Vector Error (TVE) for steady-state and dynamic situations [10]. Moreover, the synchrophasors has to be in compliance with the IEEE C37.118.2-2011 designed communication model. The design of communication has to have some critical elements including computation delay, reception and transmission speeds, functionality checks on data and the IEEE C37.118 standard data and configuration message format [11].

6. Conclusions

Hardware in the loop implementation of phasor measurement unit was achieved in this paper. This simulation was designed in Simulink and linked to the Field Programmable Gate Array coupled with an ARM microcontroller. Therefore, it has the FPGA programming logic and also able to be programmed through python for communication. The simulation was designed in the way to consider the transient of the system during and after clearing the fault. This avoids problems for protection as well as measurement components.

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